ASSIGNMENT#1

***COMPUTER ORGANIZATION AND ASSEMBLY LANGUAGE***

***WAQAS ASHIQ***

***BCS-F11-201***

***SECTION C***

***SUBMITTED TO: Sir KHAQAN ZAHEER***

***P1 TO i7***

***Alphatronic PC models P1/P2***

*This first Alphatronic computer by the German company Triumph-Adler is targeted for the business and education. The main software applications were for management, billing, word-processing (TRENDTEXT), calculation, etc...   
  
The Alphatronic uses the MOS (Micro Operating System) operating system.   
  
There were in fact two models available: P1 and P2. The Alphatronic PC/P1 had one floppy drive, and the PC/P2 had two. The picture beside seems to be a PC/P2.   
  
There was SKS/BASIC on Disc, start able by MOS directly. It was a pure Microsoft BASIC, comparable to GW-BASIC without Graphics.   
  
There was a modified version of CP/M 2.2 for this machine, and for this you could get BASIC 80 and the Siemens Macro ASSEMBLER.   
  
The native double disk-drives (160 KB each) could be replaced by higher capacity ones (785 KB each). A hard-disk (5 MB) was also available, as well as a memory expansion (64 KB).*

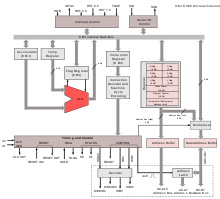
|  |  |
| --- | --- |
| *NAME* | *Alphatronic PC models P1/P2* |
| *MANUFACTURER* | *Triumph Adler* |
| *TYPE* | *Professional Computer* |
| *ORIGIN* | *Germany* |
| *YEAR* | *1980* |
| *END OF PRODUCTION* | *Unknown* |
| *BUILT IN LANGUAGE* | *Basic 80, Fortran and Pascal delivered on disk* |
| *KEYBOARD* | *Full-stroke keyboard with numeric keypad* |
| *CPU* | *8085A* |
| *SPEED* | *Unknown* |
| *CO-PROCESSOR* | *Unknown* |
| *RAM* | *48 kb, upgradable to 64 kb* |
| *VRAM* | *Unknown* |
| *ROM* | *Unknown* |
| *TEXT MODES* | *80 x 24* |
| *GRAPHIC MODES* | *Unknown* |
| *COLOrsc* | *Unknown* |
| *SOUND* | *Unknown* |
| *SIZE / WEIGHT* | *Unknown* |
| *I/O PORTS* | *V24/RS232c, IEEE48 port* |
| *BUILT IN MEDIA* | *2 x 5''1/4 disk-drives (160 kb each)* |
| *OS* | *MOS (Micro Operating System)* |
| *POWER SUPPLY* | *PSU built-in* |
| *PERIPHERALS* | *Memory expansion (64k), 2 alternative disk-drives (785kb each), Hard-disk (5Mb)* |
| *PRICE* | *5008 http://www.old-computers.com/site/graphs/euro.gif (France, 1981)* |

*The Intel 8085 is an*[*8-bit*](http://en.wikipedia.org/wiki/8-bit)[*microprocessor*](http://en.wikipedia.org/wiki/Microprocessor)*introduced by*[*Intel*](http://en.wikipedia.org/wiki/Intel)*in 1977. It was*[*binary compatible*](http://en.wikipedia.org/wiki/Binary_compatible)*with the more-famous*[*Intel 8080*](http://en.wikipedia.org/wiki/Intel_8080)*but required less supporting hardware, thus allowing simpler and less expensive*[*microcomputer*](http://en.wikipedia.org/wiki/Microcomputer)*systems to be built.*

*The "5" in the model number came from the fact that the 8085 requires only a +5-*[*volt*](http://en.wikipedia.org/wiki/Volt)*(V) power supply rather than the +5V, −5V and +12V supplies the 8080 needed. Both processors were sometimes used in computers running the*[*CP/M operating system*](http://en.wikipedia.org/wiki/CP/M_operating_system)*, and the 8085 also saw use as a microcontroller, by virtue of its low component count. Both designs were eclipsed for desktop computers by the compatible*[*Zilog Z80*](http://en.wikipedia.org/wiki/Zilog_Z80)*, which took over most of the CP/M computer market as well as taking a share of the booming*[*home computer*](http://en.wikipedia.org/wiki/Home_computer)*market in the early-to-mid-1980s.*

*The 8085 had a long life as a controller. Once designed into such products as the*[*DEC tape*](http://en.wikipedia.org/wiki/DECtape)*controller and the*[*VT100*](http://en.wikipedia.org/wiki/VT100)*video terminal in the late 1970s, it served for new production throughout the life span of those products (generally longer than the product life of desktop computers).*

i8085 microarchitecture.

*[](http://en.wikipedia.org/wiki/File:Intel_8085_arch.svg)*

***Description:***

*The 8085 is a conventional*[*von Neumann*](http://en.wikipedia.org/wiki/Von_Neumann_architecture)*design based on the Intel 8080. Unlike the 8080 it does not multiplex state signals onto the data bus, but the 8-bit*[*data bus*](http://en.wikipedia.org/wiki/Data_bus)*was instead multiplexed with the lower part of the 16-bit*[*address bus*](http://en.wikipedia.org/wiki/Address_bus)*to limit the number of pins to 40. Pin No. 40 is used for the power supply (+5v) and pin No. 20 for ground. Pin No. 39 is used as the hold pin. Pins No. 15 to No. 8 are generally used for address buses. The processor was designed using*[*nMOS*](http://en.wikipedia.org/wiki/NMOS_logic)*circuitry and the later "H" versions were implemented in Intel's enhanced nMOS process called HMOS, originally developed for fast static RAM products. Only a 5 Volt supply is needed, like competing processors and unlike the 8080. The 8085 uses approximately 6,500*[*transistors*](http://en.wikipedia.org/wiki/Transistor)*.*

*The 8085 incorporates the functions of the 8224 (clock generator) and the 8228 (system controller), increasing the level of integration. A downside compared to similar contemporary designs (such as the Z80) was the fact that the buses required DE multiplexing; however, address latches in the Intel 8155, 8355, and 8755 memory chips allowed a direct interface, so an 8085 along with these chips was almost a complete system.*

***Programming model:***

*The processor has seven 8-bit*[*registers*](http://en.wikipedia.org/wiki/Processor_register)*accessible to the programmer, named A, B, C, D, E, H, and L, where A is the 8-bit accumulator and the other six can be used as independent byte-registers or as three 16-bit register pairs, BC, DE, and HL, depending on the particular instruction. Some instructions use HL as a (limited) 16-bit accumulator. As in the 8080, the contents of the memory address pointed to by HL could be accessed as pseudo register M. It also has a 16-bit*[*stack pointer*](http://en.wikipedia.org/wiki/Stack-based_memory_allocation)*to memory (replacing the 8008's internal*[*stack*](http://en.wikipedia.org/wiki/Stack_(data_structure))*) this register is always decremented/incremented by 2 during push and pop and a 16-bit*[*program counter*](http://en.wikipedia.org/wiki/Program_counter)*. HL pair is called the primary data pointers.*

***Commands/instructions:***

*As in many other 8-bit processors, all instructions are encoded in a single byte (including register-numbers, but excluding immediate data), for simplicity. Some of them are followed by one or two bytes of data, which could be an immediate operand, a memory address, or a port number. Like larger processors, it has CALL and RET instructions for multi-level procedure calls and returns (which can be conditionally executed, like jumps) and instructions to save and restore any 16-bit register-pair on the machine stack. There are also eight one-byte call instructions (RST) for subroutines located at the fixed addresses 00h, 08h, 10h,...,38h. These were intended to be supplied by external hardware in order to invoke a corresponding interrupt-service routine, but are also often employed as fast system calls. The most sophisticated command was XTHL, which is used for exchanging the register pair HL with the value stored at the address indicated by the stack pointer.*

***8-bit instructions:***

*Most 8-bit operations work on the 8-bit*[*accumulator*](http://en.wikipedia.org/wiki/Accumulator_(computing))*(the A register). For two operand 8-bit operations, the other operand can be an immediate value, another 8-bit register, or a memory cell addressed by the 16-bit register pair HL. Direct copying is supported between any two 8-bit registers and between any 8-bit register and a HL-addressed memory cell. Due to the regular encoding of the MOV-instruction (using a quarter of available opcode space) there are redundant codes to copy a register into itself (MOV B,B, for instance), which are of little use, except for delays. However, what would have been a copy from the HL-addressed cell into itself (i.e., MOV M,M) instead encodes the*[*HLT*](http://en.wikipedia.org/wiki/HLT)*instruction, halting execution until an external reset or interrupt occurred.*

***16-bit operations:***

*Although the 8085 is an 8-bit processor, it also has some 16-bit operations. Any of the three 16-bit register pairs (BC, DE, HL) or SP could be loaded with an immediate 16-bit value (using LXI), incremented or decremented (using INX and DCX), or added to HL (using DAD). LHLD loaded HL from directly-addressed memory and SHLD stored HL likewise. The XCHG operation exchanges the values of HL and DE. Adding HL to itself performs a 16-bit arithmetical left shift with one instruction. The only 16 bit instruction that affects any flag was DAD (adding HL to BC, DE, HL or SP), which updates the carry flag to facilitate 24-bit or larger additions and left shifts (for a*[*floating point*](http://en.wikipedia.org/wiki/Floating_point)[*mantissa*](http://en.wikipedia.org/wiki/Mantissa_of_a_floating_point_number)*for instance). Adding the stack pointer to HL is useful for indexing variables in (recursive) stack frames. A stack frame can be allocated using DAD SP and SPHL, and a branch to a computed pointer can be done with PCHL. These abilities make it feasible to compile languages such as*[*PL/M*](http://en.wikipedia.org/wiki/PL/M)*,*[*Pascal*](http://en.wikipedia.org/wiki/Pascal_(programming_language))*, or*[*C*](http://en.wikipedia.org/wiki/C_(programming_language))*with 16-bit variables and produce 8085 machine code.*

***Input/output scheme:***

*The 8085 supported up to 256*[*input/output*](http://en.wikipedia.org/wiki/Input/output)*(I/O) ports, accessed via dedicated Input/output instructions—taking port addresses as operands. This Input/output mapping scheme was regarded as an advantage, as it freed up the processor's limited address space.*

***Development system:***

*Intel produced a series of development systems for the 8080 and 8085, known as the MDS-80 Microprocessor System. The original development system had an 8080 processor. Later 8085 and 8086 support was added including ICE (*[*in-circuit emulators*](http://en.wikipedia.org/wiki/In-circuit_emulator)*). It was a large and heavy desktop box, about a 20" cube (in the Intel corporate blue color) which included a CPU, monitor, and a single 8 inch floppy disk drive. Later an external box was available with two more floppy drives. It ran the*[*ISIS*](http://en.wikipedia.org/wiki/ISIS_(operating_system))*operating system and could also operate an*[*emulator*](http://en.wikipedia.org/wiki/Emulator)*pod and an external*[*EPROM*](http://en.wikipedia.org/wiki/EPROM) *programmer. This unit used the Multibus card cage which was intended just for the development system. A surprising number of spare card cages and processors were being sold, leading to the development of the Multibus as a separate product.*

***Applications:***

*For the extensive use of 8085 in various applications, the microprocessor is provided with an instruction set which consists of various instructions such as MOV, ADD, SUB, JMP, etc. These instructions are written in the form of a program which is used to perform various operations such as branching, addition, subtraction,*[*bitwise logical*](http://en.wikipedia.org/wiki/Bitwise_operation)*and*[*bit shift*](http://en.wikipedia.org/wiki/Bit_shifting)*operations. More complex operations and other arithmetic operations must be implemented in software. For example, multiplication is implemented using a*[*multiplication algorithm*](http://en.wikipedia.org/wiki/Multiplication_algorithm)*.*

***Intel Corp Pentium Family***

***Pentium:***

*Family of microprocessors developed by Intel Corp. Introduced in 1993 as the successor to Intel's 80486 microprocessor, the Pentium contained two processors on a single chip and about 3.3 million transistors. Using a CISC (complex instruction set computer) architecture, its main features were a 32-bit address bus, a 64-bit data bus, built-in floating-point and memory-management units, and two 8KB caches. It was available with processor speeds ranging from 60 megahertz (MHz) to 200 MHz The Pentium quickly became the processor of choice for personal computers. It was superseded by ever faster and more powerful processors, the Pentium Pro (1995), the Pentium II (1997), the Pentium III (1999), and the Pentium 4 (2000).*

***Pentium 4 Dual Cores - Introduced in 2005:***

*The Pentium D and Pentium Processor Extreme Edition were the first dual-core Pentium chips from Intel and the last of the Pentium line. Although both chips included Intel's 64-bit EM64T technology (later named "Intel 64"), the Pentium D did not include Hyper-Threading, but the Extreme Edition did. See Pentium Processor Extreme Edition.*

***Pentium 4 - Introduced in 2000 (1.4-3.4 GHz):***

*Latest Pentium architecture started out with a 400 MHz system bus and 256KB L2 cache (later increased to 800 MHz and 2MB). The first models contained 42 million transistors, used the 0.18 micron process and came in 423-pin and 478-pin PGA packages. Intel's first Pentium 4 chipset was the 850 and supported only Rambus memory (RDRAM), but subsequent chipsets switched to DDR SDRAM.*

***Celeron - Introduced in 1998 (266 MHz-2.8 GHz):***

*Less expensive Pentium chips due to smaller L2 caches. First Celerons had no L2 cache, but 128KB on-die cache was added in 1999. Celerons started out with 66 and 100 MHz system buses that migrated to 400 MHz*

***Pentium III - 1999-2001 (500 MHz-1.13 GHz):***

*The Pentium III added 70 additional instructions to the Pentium II. The Pentium III used a 100 or 133 MHz system bus and either a 512KB L2 cache or a 256KB L2 Advanced Transfer Cache. Depending on the model, it contained from 9.5 to 28 million transistors, used the 0.25 or 0.18 micron process and came in SECC and SECC2 packages. Mobile units came in BGA and micro-PGA (µPGA) packages.*

***Pentium III Xeon - 1999-2001 (500-933 MHz):***

*Typically used in 2-way to 8-way servers, Xeon specs were like Pentium III with L2 cache up to 2MB. The Xeon used the SECC2 and SC330 chip packages.*

***Pentium II - 1997-1999 (233-450 MHz):***

*Added MMX multimedia instructions to Pentium Pro and introduced the Single Edge Connector Cartridge (SECC) for Slot 1. The Pentium II used a 66 or 100 MHz system bus. Desktop models had 7.5 million transistors, 512KB L2 cache and were housed in SECC packages. Mobile models had 27.4 million transistors, 256KB L2 cache and were housed in either BGA or Mobile Mini-Cartridge (MMC) packages.*

***Pentium II Xeon - 1998-1999 (400-450 MHz):***

*Typically used in high-end and 2-way and 4-way servers, Xeon specs were like Pentium II with L2 cache from 512KB to 2MB and 100 MHz system bus.*

***Pentium Pro - 1995-1997 (150-200 MHz):***

*Typically used in high-end desktops and servers, the Pentium Pro increased memory from 4GB to 64GB. The Pentium Pro had L2 cache from 512KB to 1MB, used a 60 or 66 MHz system bus, contained from 5.5 to 62 million transistors. It was made with 0.35 process and housed in a dual cavity PGA package. When introduced, it was touted as being superior to the Pentium for 32-bit applications.*

***Pentium MMX - 1997-1999 (233-300 MHz):***

*Added MMX multimedia instructions to Pentium CPU and increased transistors to 4.5 million. Desktop units used PGA package and 0.35 process while mobile units used TCP and 0.25 process.*

***Pentium - 1993-1996 (60-200 MHz):***

*First Pentium CPU models. The Pentium had an L2 cache from 256KB to 1MB, used a 50, 60 or 66 MHz system bus and contained from 3.1 to 3.3 million transistors built on 0.6 to 0.35 process. Chips were housed in PGA packages.*

***Intel Core family***

***Intel Core****is a brand name used for various mid-range to high-end consumer and business*[*microprocessors*](http://en.wikipedia.org/wiki/Microprocessors)*made by*[*Intel*](http://en.wikipedia.org/wiki/Intel)*.*

*The current lineup of Core processors includes the latest*[*Intel Core i7*](http://en.wikipedia.org/wiki/Intel_Core#Core_i7)*,*[*Intel Core i5*](http://en.wikipedia.org/wiki/Intel_Core#Core_i5)*, and*[*Intel Core i3*](http://en.wikipedia.org/wiki/Intel_Core#Core_i3)*, and the older*[*Intel Core 2 Solo*](http://en.wikipedia.org/wiki/Intel_Core#Core_2_Solo)*,*[*Intel Core 2 Duo*](http://en.wikipedia.org/wiki/Intel_Core#Core_2_Duo)*,*[*Intel Core 2 Quad*](http://en.wikipedia.org/wiki/Intel_Core#Core_2_Quad)*, and Intel core 2.*

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| ***Brand*** | [***Desktop***](http://en.wikipedia.org/wiki/Desktop_computer) | | | | [***Laptop***](http://en.wikipedia.org/wiki/Laptop) | | | |
| ***Code-named*** | ***Cores*** | ***Fab*** | ***Date released*** | ***Code-named*** | ***Cores*** | ***Fab*** | ***Date released*** |
| ***Core Solo*** | *Desktop version not available* | | | | [*Yonah*](http://en.wikipedia.org/wiki/Yonah_(microprocessor)) | *1* | *65 nm* | *January 2006* |
| ***Core Duo*** | *Desktop version not available* | | | | [*Yonah*](http://en.wikipedia.org/wiki/Yonah_(microprocessor)) | *2* | *65 nm* | *January 2006* |
| ***Core 2 Solo*** | *Desktop version not available* | | | | [*Merom-L*](http://en.wikipedia.org/wiki/Merom_(microprocessor)#Merom-L)[*Penryn-L*](http://en.wikipedia.org/wiki/Penryn_(microprocessor)#Penryn) | *1 1* | *65 nm 45 nm* | *September 2007 May 2008* |
| ***Core 2 Duo*** | [*Conroe*](http://en.wikipedia.org/wiki/Conroe_(microprocessor)#Conroe)[*Allendale*](http://en.wikipedia.org/wiki/Conroe_(microprocessor)#Allendale)[*Wolfdale*](http://en.wikipedia.org/wiki/Wolfdale_(microprocessor)) | *2 2 2* | *65 nm 65 nm 45 nm* | *August 2006 January 2007 January 2008* | [*Merom*](http://en.wikipedia.org/wiki/Merom_(microprocessor))[*Penryn*](http://en.wikipedia.org/wiki/Penryn_(microprocessor)) | *2 2* | *65 nm 45 nm* | *July 2006 January 2008* |
| ***Core 2 Quad*** | [*Kentsfield*](http://en.wikipedia.org/wiki/Kentsfield_(microprocessor))[*Yorkfield*](http://en.wikipedia.org/wiki/Yorkfield_(microprocessor)) | *4 4* | *65 nm 45 nm* | *January 2007 March 2008* | [*Penryn*](http://en.wikipedia.org/wiki/Penryn_(microprocessor)) | *4* | *45 nm* | *August 2008* |
| ***Core 2 Extreme*** | [*Conroe XE*](http://en.wikipedia.org/wiki/Conroe_(microprocessor)#Conroe_XE)[*Kentsfield XE*](http://en.wikipedia.org/wiki/Kentsfield_(microprocessor)#Kentsfield_XE)[*Yorkfield XE*](http://en.wikipedia.org/wiki/Yorkfield_(microprocessor)#Yorkfield_XE) | *2 4 4* | *65 nm 65 nm 45 nm* | *July 2006 November 2006 November 2007* | [*Merom XE*](http://en.wikipedia.org/wiki/Merom_(microprocessor)#Merom_XE)[*Penryn XE*](http://en.wikipedia.org/wiki/Penryn_(microprocessor)#Penryn_XE)[*Penryn XE*](http://en.wikipedia.org/wiki/Penryn_(microprocessor)#Penryn_QC) | *2 2 4* | *65 nm 45 nm 45 nm* | *July 2007 January 2008 August 2008* |
| ***Core i3*** | [*Clarkdale*](http://en.wikipedia.org/wiki/Clarkdale_(microprocessor))[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor)) | *2 2 2* | *32 nm 32 nm 22 nm* | *January 2010 February 2011 Q3 2012* | [*Arrandale*](http://en.wikipedia.org/wiki/Arrandale_(microprocessor))[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor)) | *2 2 2* | *32 nm 32 nm 22 nm* | *January 2010 February 2011 June 2012* |
| ***Core i5*** | [*Lynnfield*](http://en.wikipedia.org/wiki/Lynnfield_(microprocessor))[*Clarkdale*](http://en.wikipedia.org/wiki/Clarkdale_(microprocessor))[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor))[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor)) | *4 2 4 2 4 2* | *45 nm 32 nm 32 nm 32 nm 22 nm 22 nm* | *September 2009 January 2010 January 2011 February 2011 April 2012 April 2012* | [*Arrandale*](http://en.wikipedia.org/wiki/Arrandale_(microprocessor))[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor)) | *2 2 2* | *32 nm 32 nm 22 nm* | *January 2010 February 2011 May 2012* |
| ***Core i7*** | [*Bloomfield*](http://en.wikipedia.org/wiki/Bloomfield_(microprocessor))[*Lynnfield*](http://en.wikipedia.org/wiki/Lynnfield_(microprocessor))[*Gulftown*](http://en.wikipedia.org/wiki/Gulftown_(microprocessor))[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor)) | *4 4 6 4 4* | *45 nm 45 nm 32 nm 32 nm 22 nm* | *November 2008 September 2009 July 2010 January 2011 April 2012* | [*Clarksfield*](http://en.wikipedia.org/wiki/Clarksfield_(microprocessor))[*Arrandale*](http://en.wikipedia.org/wiki/Arrandale_(microprocessor))[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor)) | *4 2 4 2 2* | *45 nm 32 nm 32 nm 32 nm 22 nm* | *September 2009 January 2010 January 2011 February 2011 May 2012* |
| ***Core i7 Extreme Edition*** | [*Bloomfield*](http://en.wikipedia.org/wiki/Bloomfield_(microprocessor))[*Gulftown*](http://en.wikipedia.org/wiki/Gulftown_(microprocessor))[*Sandy Bridge-E*](http://en.wikipedia.org/wiki/Sandy_Bridge) | *4 6 6* | *45 nm 32 nm 32 nm* | *November 2008 March 2010 November 2011* | [*Clarksfield*](http://en.wikipedia.org/wiki/Clarksfield_(microprocessor))[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor)) | *4 4 4* | *45 nm 32 nm 22 nm* | *September 2009 January 2011 May 2012* |
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### *Core Duo*

***Intel Core Duo****(product code 80539) consists of two cores on one die, a 2*[*MB*](http://en.wikipedia.org/wiki/Megabyte)*L2 cache shared by both cores, and an arbiter bus that controls both L2 cache and FSB (front-side bus) access.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***L2 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) |
| [***Yonah***](http://en.wikipedia.org/wiki/Yonah_(microprocessor)) | [*Core Duo T2xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_microprocessors#.22Yonah.22_.28standard-voltage.2C_65_nm.29) | *2 MB* | [*Socket M*](http://en.wikipedia.org/wiki/Socket_M) | *31 W* |
| [*Core Duo L2xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_microprocessors#.22Yonah.22_.28low-voltage.2C_65_nm.29) | *15 W* |
| [*Core Duo U2xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_microprocessors#.22Yonah.22_.28ultra_low-voltage.2C_65_nm.29) | *9 W* |

### *Core Solo*

***Intel Core Solo****(product code 80538) uses the same two-core die as the Core Duo, but features only one active core. Depending on demand, Intel may also simply disable one of the cores to sell the chip at the Core Solo price—this requires less effort than launching and maintaining a separate line of CPUs that physically only have one core. Intel used the same strategy previously with the*[*486*](http://en.wikipedia.org/wiki/Intel_80486)*CPU in which early*[*486SX*](http://en.wikipedia.org/wiki/486SX)*CPUs were in fact manufactured as*[*486DX*](http://en.wikipedia.org/wiki/486DX)*CPUs but with the*[*FPU*](http://en.wikipedia.org/wiki/Floating_point_unit)*disabled.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***L2 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) |
| [***Yonah***](http://en.wikipedia.org/wiki/Yonah_(microprocessor)) | [*Core Solo T1xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_microprocessors#.22Yonah.22_.28standard_voltage.2C_65_nm.29) | *2 MB* | [*Socket M*](http://en.wikipedia.org/wiki/Socket_M) | *27–31 W* |
| [*Core Solo U1xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_microprocessors#.22Yonah.22_.28ultra-low-voltage.2C_65_nm.29) | *5.5–6 W* |

### *Core 2 Solo*

*The****Core 2 Solo****introduced in September 2007, is the successor to the Core Solo and is available only as an ultra-low-power mobile processor with 5.5 Watt thermal design power. The original U2xxx series "Merom-L" used a special version of the Merom chip with*[*CPUID*](http://en.wikipedia.org/wiki/CPUID)*number 10661 (model 22, stepping A1) that only had a single core and was also used in some Celeron processors. The later SU3xxx are part of Intel's*[*CULV*](http://en.wikipedia.org/wiki/CULV)*range of processors in a smaller µFC-BGA 956 package but contain the same Penryn chip as the dual-core variants, with one of the cores disabled during manufacturing.*

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| --- | --- | --- | --- | --- |
| ***Codename (main article)*** | ***Brand name (list)*** | ***L2 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) |
| [***Merom-L***](http://en.wikipedia.org/wiki/Merom_(microprocessor)#Merom-L) | [*Mobile Core 2 Solo U2xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Merom-L.22_.28ultra-low-voltage.2C_65_nm.29) | *1 MB* | *FCBGA* | *5.5 W* |
| [***Penryn-L***](http://en.wikipedia.org/wiki/Penryn_(microprocessor)#Penryn-L) | [*Mobile Core 2 Solo SU3xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn-L.22_.28ultra-low-voltage.2C_45_nm.2C_Small_Form_Factor.29) | *3 MB* | *BGA956* | *5.5 W* |

### *Core 2 Duo*

*The majority of the desktop and mobile Core 2 processor variants are****Core 2 Duo****with two processor cores on a single [Merom](http://en.wikipedia.org/wiki/Merom_(microprocessor)" \o "Merom (microprocessor)),*[*Conroe*](http://en.wikipedia.org/wiki/Conroe_(microprocessor))*,*[*Allendale*](http://en.wikipedia.org/wiki/Conroe_(microprocessor)#Allendale)*, [Penryn](http://en.wikipedia.org/wiki/Penryn_(microprocessor)" \o "Penryn (microprocessor)), or [Wolfdale](http://en.wikipedia.org/wiki/Wolfdale_(microprocessor)" \o "Wolfdale (microprocessor)) chip. These come in a wide range of performance and power consumption, starting with the relatively slow ultra-low-power Uxxxx (10 W) and low-power Lxxxx (17 W) versions, to the more performance oriented Pxxxx (25 W) and Txxxx (35 W) mobile versions and the Exxxx (65 W) desktop models. The mobile Core 2 Duo processors with an 'S' prefix in the name are produced in a smaller µFC-BGA 956 package, which allows building more compact laptops.*

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| [***Merom***](http://en.wikipedia.org/wiki/Merom_(microprocessor)) | [*Mobile Core 2 Duo U7xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Merom.22_.28ultra-low-voltage.2C_65_nm.29) | *2 MB* | *BGA479* | *10 W* |
| [*Mobile Core 2 Duo L7xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Merom.22_.28low-voltage.2C_65_nm.29) | *4 MB* | *17 W* |
| [*Mobile Core 2 Duo T5xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Merom.22.2C_.22Merom-2M.22_.28standard-voltage.2C_65_nm.29) | *2 MB* | [*Socket M*](http://en.wikipedia.org/wiki/Socket_M)[*Socket P*](http://en.wikipedia.org/wiki/Socket_P) *BGA479* | *35 W* |
| [*Mobile Core 2 Duo T7xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Merom.22.2C_.22Merom-2M.22_.28standard-voltage.2C_65_nm.29) | *2–4 MB* |
| [***Conroe and Allendale***](http://en.wikipedia.org/wiki/Conroe_(microprocessor)) | [*Core 2 Duo E4xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Allendale.22_.2865_nm.29) | *2 MB* | [*LGA 775*](http://en.wikipedia.org/wiki/LGA_775) | *65 W* |
| [*Core 2 Duo E6xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Conroe.22_.2865_nm.29) | *2–4 MB* |
| [***Penryn***](http://en.wikipedia.org/wiki/Penryn_(microprocessor)) | [*Mobile Core 2 Duo SU7xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn-3M.22_.28ultra-low-voltage.2C_45_nm.2C_Small_Form_Factor.29) | *3 MB* | *BGA956* | *10W* |
| [*Mobile Core 2 Duo SU9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn-3M.22_.28ultra-low-voltage.2C_45_nm.2C_Small_Form_Factor.29) |
| [*Mobile Core 2 Duo SL9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28low-voltage.2C_45_nm.2C_Small_Form_Factor.29) | *6 MB* | *17 W* |
| [*Mobile Core 2 Duo SP9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28medium-voltage.2C_45_nm.2C_Small_Form_Factor.29) | *25 W* |
| [*Mobile Core 2 Duo P7xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28medium-voltage.2C_45_nm.29) | *3 MB* | [*Socket P*](http://en.wikipedia.org/wiki/Socket_P) *FCBGA6* | *25 W* |
| [*Mobile Core 2 Duo P8xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28medium-voltage.2C_45_nm.29) |
| [*Mobile Core 2 Duo P9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28medium-voltage.2C_45_nm.29) | *6 MB* |
| [*Mobile Core 2 Duo T6xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28standard-voltage.2C_45_nm.29) | *2 MB* | *35 W* |
| [*Mobile Core 2 Duo T8xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28standard-voltage.2C_45_nm.29) | *3 MB* |
| [*Mobile Core 2 Duo T9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28standard-voltage.2C_45_nm.29) | *6 MB* |
| [*Mobile Core 2 Duo E8xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn.22_.28Apple_iMac_specific.2C_45_nm.29) | *6 MB* | *Socket P* | *35-55 W* |
| [***Wolfdale***](http://en.wikipedia.org/wiki/Wolfdale_(microprocessor)) | [*Core 2 Duo E7xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Wolfdale-3M.22_.2845_nm.29) | *3 MB* | [*LGA 775*](http://en.wikipedia.org/wiki/LGA_775) | *65 W* |
| [*Core 2 Duo E8xxx*](http://en.wikipedia.org/wiki/E8500) | *6 MB* |

### *Core 2 Quad*

***Core 2 Quad****processors are*[*multi-chip modules*](http://en.wikipedia.org/wiki/Multi-chip_module)*consisting of two dies similar to those used in Core 2 Duo, forming a quad-core processor. This allows twice the performance of a dual-core processors at the same clock frequency in ideal conditions.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***L2 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) |
| [***Kentsfield***](http://en.wikipedia.org/wiki/Kentsfield_(microprocessor)) | [*Core 2 Quad Q6xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Kentsfield.22_.2865_nm.29) | *2×4 MB* | [*LGA 775*](http://en.wikipedia.org/wiki/LGA_775) | *95–105 W* |
| [***Yorkfield***](http://en.wikipedia.org/wiki/Yorkfield_(microprocessor)) | [*Core 2 Quad Q7xxx*](http://en.wikipedia.org/wiki/Q9400) | *2×1 MB* | *95 W* |
| [*Core 2 Quad Q8xxx*](http://en.wikipedia.org/wiki/Q9400) | *2×2 MB* | *65–95 W* |
| [*Core 2 Quad Q9xxx*](http://en.wikipedia.org/wiki/Q9450) | *2×3–2×6 MB* |
| [***Penryn-QC***](http://en.wikipedia.org/wiki/Penryn_(microprocessor)#Penryn-QC) | [*Mobile Core 2 Quad Q9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn_QC.22_.28standard-voltage.2C_45_nm.29) | *2×3–2×6 MB* | *Socket P* | *45 W* |

### *Core 2 Extreme*

***Core 2 Extreme****processors are enthusiast versions of Core 2 Duo and Core 2 Quad processors, usually with a higher clock frequency and an unlocked*[*clock multiplier*](http://en.wikipedia.org/wiki/CPU_multiplier)*, which makes them especially attractive for*[*overclocking*](http://en.wikipedia.org/wiki/Overclocking)*. This is similar to earlier*[*Pentium*](http://en.wikipedia.org/wiki/Pentium_(brand))*processors labeled as*[*Extreme Edition*](http://en.wikipedia.org/wiki/Extreme_Edition)*. Core 2 Extreme processors were released at a much higher price than their regular version, often $999 or more.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***L2 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) |
| [***Merom***](http://en.wikipedia.org/wiki/Merom_(microprocessor)) | [*Mobile Core 2 Extreme X7xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Merom_XE.22_.28standard-voltage.2C_65_nm.29) | *4 MB* | [*Socket P*](http://en.wikipedia.org/wiki/Socket_P) | *44 W* |
| [***Conroe***](http://en.wikipedia.org/wiki/Conroe_(microprocessor)) | [*Core 2 Extreme X6xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Conroe_XE.22_.2865_nm.29) | *4 MB* | [*LGA 775*](http://en.wikipedia.org/wiki/LGA_775) | *75 W* |
| [***Kentsfield***](http://en.wikipedia.org/wiki/Kentsfield_(microprocessor)) | [*Core 2 Extreme QX6xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Kentsfield_XE.22_.2865_nm.29) | *2×4 MB* | *LGA 775* | *130 W* |
| [***Penryn***](http://en.wikipedia.org/wiki/Penryn_(microprocessor)) | [*Mobile Core 2 Extreme X9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn_XE.22_.28standard-voltage.2C_45_nm.29) | *6 MB* | *Socket P* | *44 W* |
| [***Penryn-QC***](http://en.wikipedia.org/wiki/Penryn_(microprocessor)#Penryn-QC) | [*Mobile Core 2 Extreme QX9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Penryn_QC_XE.22_.28standard-voltage.2C_45_nm.29) | *2×6 MB* | *Socket P* | *45 W* |
| [***Yorkfield***](http://en.wikipedia.org/wiki/Yorkfield_(microprocessor)) | [*Core 2 Extreme QX9xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_2_microprocessors#.22Yorkfield_XE.22_.2845_nm.29) | *2×6 MB* | *LGA 775 / LGA 771* | *130–150 W* |

### *Core i3*

*The****Core i3****was intended to be the new low end of the performance processor line from*[*Intel*](http://en.wikipedia.org/wiki/Intel)*, following the retirement of the*[*Core 2*](http://en.wikipedia.org/wiki/Intel_Core_2)*brand.*

*The first Core i3 processors were launched on January 7, 2010.*

*The first Nehalem based Core i3 was*[*Clarkdale*](http://en.wikipedia.org/wiki/Clarkdale_(microprocessor))*-based, with an integrated*[*GPU*](http://en.wikipedia.org/wiki/GPU)*and two cores. The same processor is also available as Core i5 and Pentium, with slightly different configurations.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***Cores*** | ***L3 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) | ***I/O Bus*** |
| [***Clarkdale***](http://en.wikipedia.org/wiki/Clarkdale_(microprocessor)) | [*Core i3-5xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Clarkdale.22_.2832_nm.29) | *2* | *4 MB* | [*LGA 1156*](http://en.wikipedia.org/wiki/LGA_1156) | *73 W* | [*Direct Media Interface*](http://en.wikipedia.org/wiki/Direct_Media_Interface)*, Integrated*[*GPU*](http://en.wikipedia.org/wiki/Graphics_processing_unit) |
| [***Arrandale***](http://en.wikipedia.org/wiki/Arrandale_(microprocessor)) | [*Core i3-3xxM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Arrandale.22_.2832_nm.29) | *3 MB* | [*rPGA-988A*](http://en.wikipedia.org/wiki/Socket_G1) | *35 W* |
| [*Core i3-3xxUM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Arrandale.22_.2832_nm.29) | *3 MB* | *BGA-1288* | *18 W* |  |

### *Core i5*

*The first****Core i5****using the*[*Nehalem*](http://en.wikipedia.org/wiki/Nehalem_(microarchitecture))*microarchitecture was introduced on September 8, 2009, as a mainstream variant of the earlier Core i7, the*[*Lynnfield*](http://en.wikipedia.org/wiki/Lynnfield_(microprocessor))*core. Lynnfield Core i5 processors have an 8 MB*[*L3 cache*](http://en.wikipedia.org/wiki/L3_cache)*, a DMI bus running at 2.5 GT/s and support for dual-channel DDR3-800/1066/1333 memory and have*[*Hyper-threading*](http://en.wikipedia.org/wiki/Hyper-threading)*disabled. The same processors with different sets of features (*[*Hyper-Threading*](http://en.wikipedia.org/wiki/Hyper-Threading)*and other clock frequencies) enabled are sold as*[*Core i7-8xx*](http://en.wikipedia.org/wiki/Intel_Core_i7)*and*[*Xeon 3400-series*](http://en.wikipedia.org/wiki/Xeon#3400-series_.22Lynnfield.22)*processors, which should not be confused with high-end Core i7-9xx and Xeon 3500-series processors based on*[*Bloomfield*](http://en.wikipedia.org/wiki/Bloomfield_(microprocessor))*.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***Cores*** | ***L3 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) | ***I/O Bus*** |
| [***Lynnfield***](http://en.wikipedia.org/wiki/Lynnfield_(microprocessor)) | [*Core i5-7xx*](http://en.wikipedia.org/wiki/Core_i5-750) | *4* | *8 MB* | [*LGA 1156*](http://en.wikipedia.org/wiki/LGA_1156) | *95 W* | [*Direct Media Interface*](http://en.wikipedia.org/wiki/Direct_Media_Interface) |
| [*Core i5-7xxS*](http://en.wikipedia.org/wiki/Core_i5-750) | *82 W* |
| [***Clarkdale***](http://en.wikipedia.org/wiki/Clarkdale_(microprocessor)) | [*Core i5-6xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Clarkdale.22_.2832_nm.29) | *2* | *4 MB* | *73–87 W* | *Direct Media Interface, Integrated*[*GPU*](http://en.wikipedia.org/wiki/Graphics_processing_unit) |
| [***Arrandale***](http://en.wikipedia.org/wiki/Arrandale_(microprocessor)) | [*Core i5-5xxM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Arrandale.22_.2832_nm.29_2) | *3 MB* | [*rPGA-988A*](http://en.wikipedia.org/wiki/Socket_G1) | *35 W* |
| [*Core i5-4xxM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Arrandale.22_.2832_nm.29_2) |
| [*Core i5-5xxUM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Arrandale.22_.2832_nm.29_2) | *BGA-1288* | *18 W* |
| [*Core i5-4xxUM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Arrandale.22_.2832_nm.29_2)[*[32]*](http://en.wikipedia.org/wiki/Intel_Core#cite_note-31) |

### *Core i7*

***Intel Core i7****is an*[*Intel*](http://en.wikipedia.org/wiki/Intel)*brand name for several families of desktop and laptop*[*64-bit*](http://en.wikipedia.org/wiki/64-bit)[*x86-64*](http://en.wikipedia.org/wiki/X86-64)*processors using the*[*Nehalem*](http://en.wikipedia.org/wiki/Nehalem_(microarchitecture))*, [Westmere](http://en.wikipedia.org/wiki/Nehalem_(microarchitecture)" \l "Westmere" \o "Nehalem (microarchitecture)),*[*Sandy Bridge*](http://en.wikipedia.org/wiki/Sandy_Bridge)*and*[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microarchitecture))[*microarchitectures*](http://en.wikipedia.org/wiki/Microarchitecture)*. The Core i7 brand is targeted at the business and high-end consumer markets for both desktop and laptop computers, and is distinguished from the*[*Core i3*](http://en.wikipedia.org/wiki/Intel_Core#Core_i3)*(entry-level consumer),*[*Core i5*](http://en.wikipedia.org/wiki/Intel_Core#Core_i5)*(mainstream consumer), and*[*Xeon*](http://en.wikipedia.org/wiki/Xeon)*(server and workstation) brands.*

*The Core i7 name was introduced with the*[*Bloomfield*](http://en.wikipedia.org/wiki/Bloomfield_(microprocessor))*Quad-core processor in late 2008. In 2009 new Core i7 models based on the*[*Lynnfield*](http://en.wikipedia.org/wiki/Lynnfield_(microprocessor))*desktop quad-core processor and the* [*Clarksfield*](http://en.wikipedia.org/wiki/Clarksfield_(microprocessor))*quad-core mobile were added, and models based on the [Arrandale](http://en.wikipedia.org/wiki/Arrandale_(microprocessor)" \o "Arrandale (microprocessor)) dual-core mobile processor were added in January 2010. The first six-core processor in the Core lineup is the* [*Gulftown*](http://en.wikipedia.org/wiki/Gulftown_(microprocessor))*, which was launched on March 16, 2010. Both the regular Core i7 and the Extreme Edition are advertised as five stars in the Intel Processor Rating. In January 2011, Intel released the second generation of Core i7 processors. Both the first and second generation of Intel Core i7 processors are rated as 5 stars in the Intel processor rating. The second generation of Intel core processors are based on the "Sandy Bridge" core and were updated in April 2012 with "Ivy Bridge".*

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| ***Code name*** | ***Brand name*** | ***Cores*** | ***L3 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) | ***Process*** | ***Busses*** | ***Release Date*** |
| [*Gulftown*](http://en.wikipedia.org/wiki/Gulftown_(microprocessor)) | [*Core i7-9xxX Extreme Edition*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Gulftown.22_.2832_nm.29) | *6* | *12 MB* | [*LGA 1366*](http://en.wikipedia.org/wiki/LGA_1366) | *130 W* | [*32 nm*](http://en.wikipedia.org/wiki/32_nanometer) | [*QPI*](http://en.wikipedia.org/wiki/QuickPath)*, 3 ×*[*DDR3*](http://en.wikipedia.org/wiki/DDR3) | *Mar 2010* |
| [*Core i7-9xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Gulftown.22_.2832_nm.29) | *Jul 2010* |
| [*Bloomfield*](http://en.wikipedia.org/wiki/Bloomfield_(microprocessor)) | [*Core i7-9xx Extreme Edition*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Bloomfield_XE.22_.2845_nm.29) | *4* | *8 MB* | [*45 nm*](http://en.wikipedia.org/wiki/45_nanometer) | *Nov 2008* |
| [*Core i7-9xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Bloomfield.22_.2845_nm.29) |
| [*Lynnfield*](http://en.wikipedia.org/wiki/Lynnfield_(microprocessor)) | [*Core i7-8xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Lynnfield.22_.2845_nm.29) | [*LGA 1156*](http://en.wikipedia.org/wiki/LGA_1156) | *95 W* | [*DMI*](http://en.wikipedia.org/wiki/Direct_Media_Interface)*,* [*PCI-e*](http://en.wikipedia.org/wiki/PCI-e)*, 2 ×*[*DDR3*](http://en.wikipedia.org/wiki/DDR3) | *Sep 2009* |
| [*Core i7-8xxS*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Lynnfield.22_.2845_nm.29) | *82 W* | *Jan 2010* |
| [*Clarksfield*](http://en.wikipedia.org/wiki/Clarksfield_(microprocessor)) | [*Core i7-9xxXM Extreme Edition*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Clarksfield_XM.22_.2845_nm.29) | [*rPGA-988A*](http://en.wikipedia.org/wiki/Socket_G1) | *55 W* | *Sep 2009* |
| [*Core i7-8xxQM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Clarksfield.22_.2845_nm.29) | *45 W* |
| [*Core i7-7xxQM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Clarksfield.22_.2845_nm.29) | *6 MB* |
| [*Arrandale*](http://en.wikipedia.org/wiki/Arrandale_(microprocessor)) | [*Core i7-6xxM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Arrandale.22_.2832_nm.29_2) | *2* | *4 MB* | *35 W* | [*32 nm*](http://en.wikipedia.org/wiki/32_nanometer) | [*DMI*](http://en.wikipedia.org/wiki/Direct_Media_Interface)*,* [*PCI-e*](http://en.wikipedia.org/wiki/PCI-e)*,* [*FDI*](http://en.wikipedia.org/wiki/Flexible_Display_Interface)*, 2 ×*[*DDR3*](http://en.wikipedia.org/wiki/DDR3) | *Jan 2010* |
| [*Core i7-6xxLM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Arrandale.22_.2832_nm.29_2) | *BGA-1288* | *25 W* |
| [*Core i7-6xxUM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Arrandale.22_.2832_nm.29_2) | *18 W* |

*In early 2011, a new microarchitecture named*[***Sandy Bridge microarchitecture***](http://en.wikipedia.org/wiki/Sandy_Bridge)*was introduced by Intel, which keeps all the existing brands from Nehalem including Core i3/i5/i7, but introduces new model numbers. The initial set of Sandy Bridge processors includes dual- and quad-core variants, all of which use a single 32 nm die for both the CPU and integrated GPU cores, unlike the earlier microarchitectures. All Core i3/i5/i7 processors with the Sandy Bridge microarchitecture have a four-digit model number. With the mobile version, the*[*thermal design power*](http://en.wikipedia.org/wiki/Thermal_design_power)*can no longer be determined from a one- or two-letter suffix but is encoded into the CPU number. Starting with Sandy Bridge, Intel no longer distinguishes the code names of the processor based on number of cores, socket or intended usage; they all use the same code name as the microarchitecture itself.*

[*Ivy Bridge*](http://en.wikipedia.org/wiki/Ivy_Bridge_(microprocessor))*is the codename for Intel's 22 nm die shrink of the Sandy Bridge microarchitecture based on tri-gate ("3D") transistors, introduced in April 2012.*

### *Core i3*

*Released on January 20, 2011, the Core i3-2xxx line of desktop and mobile processors is a direct replacement of the 2010 "Clarkdale" Core i3-5xx and "Arrandale" Core i3-3xxM models, based on the new microarchitecture. While they require new sockets and chipsets, the user-visible features of the Core i3 are largely unchanged, including the lack of support for*[*Turbo Boost*](http://en.wikipedia.org/wiki/Intel_Turbo_Boost)*and*[*AES-NI*](http://en.wikipedia.org/wiki/AES-NI)*. Unlike the Sandy Bridge based Celeron and Pentium processors, the Core i3 line does support the new*[*Advanced Vector Extensions*](http://en.wikipedia.org/wiki/Advanced_Vector_Extensions)*.*

*The Ivy Bridge based Core-i3-3xxx line is a minor upgrade to 22 nm process technology and better graphics.*

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| --- | --- | --- | --- | --- | --- | --- |
| ***Codename (main article)*** | ***Brand name (list)*** | ***Cores*** | ***L3 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) | ***I/O Bus*** |
| [***Sandy Bridge (Desktop)***](http://en.wikipedia.org/wiki/Sandy_Bridge) | [*Core i3-21xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *2* | *3 MB* | [*LGA 1155*](http://en.wikipedia.org/wiki/LGA_1155) | *65 W* | [*Direct Media Interface*](http://en.wikipedia.org/wiki/Direct_Media_Interface)*, Integrated*[*GPU*](http://en.wikipedia.org/wiki/Graphics_processing_unit) |
| [*Core i3-21xxT*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *35 W* |
| [***Sandy Bridge (Mobile)***](http://en.wikipedia.org/wiki/Sandy_Bridge) | [*Core i3-2xx0M*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_2) | *rPGA-988B BGA-1023* |
| [*Core i3-2xx7M*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_2) | *BGA-1023* | *17 W* |
| [***Ivy Bridge (Mobile)***](http://en.wikipedia.org/wiki/Ivy_Bridge_(microarchitecture)) | [*Core i3-3xx0M*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) | *rPGA-988B BGA-1023* | *35 W* |
| [*Core i3-3xx7U*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i3_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) | *BGA-1023* | *17 W* |

### *Core i5*

*In January 2011, Intel released new quad-core Core i5 processors based on the "Sandy Bridge" microarchitecture at CES 2011. New dual-core mobile processors and desktop processors arrived in February 2011.*

*The Core i5-2xxx line of desktop processors are mostly quad-core chips, with the exception of the dual-core Core i5-2390T, and include integrated graphics, combining the key features of the earlier Core i5-6xx and Core i5-7xx lines. The suffix after the four-digit model number designates unlocked multiplier (K), low-power (S) and ultra-low-power (T).*

*The desktop CPUs now all have four non-SMT cores (like the i5-750), with the exception of the i5-2390T. The DMI bus is running at 5 GT/s.*

*The mobile Core i5-2xxxM processors are all dual-core chips like the previous Core i5-5xxM series and share most the features with that product line.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***Cores*** | ***L3 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) | ***I/O Bus*** |
| [***Sandy Bridge (Desktop)***](http://en.wikipedia.org/wiki/Sandy_Bridge) | [*Core i5-2xxx Core i5-2xxxK*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_2) | *4* | *6 MB* | [*LGA 1155*](http://en.wikipedia.org/wiki/LGA_1155) | *95 W* | [*Direct Media Interface*](http://en.wikipedia.org/wiki/Direct_Media_Interface)*, Integrated*[*GPU*](http://en.wikipedia.org/wiki/Graphics_processing_unit) |
| [*Core i5-2xxxS*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_2) | *65 W* |
| [*Core i5-25xxT*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *45 W* |
| [*Core i5-23xxT*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *2* | *3 MB* | *35 W* |
| [***Ivy Bridge (Desktop)***](http://en.wikipedia.org/wiki/Ivy_Bridge_(microarchitecture)) | [*Core i5-3xxx Core i5-3xxxK*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Ivy_Bridge.22_.28quad-core.2C_22_nm.29) | *4* | *6 MB* | *77 W* |
| [*Core i5-3xxxS*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Ivy_Bridge.22_.28quad-core.2C_22_nm.29) | *65 W* |
| [*Core i5-35xxT*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Ivy_Bridge.22_.28quad-core.2C_22_nm.29) | *45 W* |
| [*Core i5-34xxT*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Ivy_Bridge.22_.28dual-core.2C_22_nm.29) | *2* | *3 MB* | *35 W* |
| [***Sandy Bridge (Mobile)***](http://en.wikipedia.org/wiki/Sandy_Bridge) | [*Core i5-2xxxM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_3) | *2* | *3 MB* | *rPGA-988B BGA-1023* | *35 W* |
| [*Core i5-2xx7M*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_3) | *BGA-1023* | *17 W* |
| [***Ivy Bridge (Mobile)***](http://en.wikipedia.org/wiki/Ivy_Bridge_(microarchitecture)) | [*Core i5-3xx0M*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) | *rPGA-988B BGA-1023* | *35 W* |
| [*Core i5-3xx7U*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i5_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) | *BGA-1023* | *17 W* |

### *Core i7*

*The Core i7 brand remains the high-end for Intel's desktop and mobile processors, featuring the Sandy Bridge models with the largest amount of L3 cache and the highest clock frequency. Most of these models are very similar to their smaller Core i5 siblings. The quad-core mobile Core i7-2xxxQM/XM processors follow the previous "Clarksfield" Core i7-xxxQM/XM processors, but now also include integrated graphics.*

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| ***Codename (main article)*** | ***Brand name (list)*** | ***Cores*** | ***L3 Cache*** | ***Socket*** | [***TDP***](http://en.wikipedia.org/wiki/Thermal_design_power) | ***Process*** | ***I/O Bus*** | ***Release Date*** |
| [***Ivy Bridge (Desktop)***](http://en.wikipedia.org/wiki/Ivy_Bridge_(microarchitecture)) | [*Core i7-37xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) | *4* | *8 MB* | [*LGA 1155*](http://en.wikipedia.org/wiki/LGA_1155) | *77 W* | [*22 nm*](http://en.wikipedia.org/wiki/22_nanometer) | [*Direct Media Interface*](http://en.wikipedia.org/wiki/Direct_Media_Interface)*, Integrated*[*GPU*](http://en.wikipedia.org/wiki/Graphics_processing_unit) | *April 2012* |
| [*Core i7-37xxK*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) |
| [*Core i7-37xxS*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) | *65 W* |
| [*Core i7-37xxT*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Ivy_Bridge.22_.2822_nm.29) | *45 W* |
| [***Sandy Bridge-E (Desktop)***](http://en.wikipedia.org/wiki/Sandy_Bridge-E) | [*Core i7-39xxX*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *6* | *15 MB* | [*LGA 2011*](http://en.wikipedia.org/wiki/LGA_2011) | *130 W* | [*32 nm*](http://en.wikipedia.org/wiki/32_nanometer) | [*Direct Media Interface*](http://en.wikipedia.org/wiki/Direct_Media_Interface) | *November 2011* |
| [*Core i7-39xxK*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *12 MB* |
| [*Core i7-38xx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *4* | *10 MB* |
| [***Sandy Bridge (Desktop)***](http://en.wikipedia.org/wiki/Sandy_Bridge) | [*Core i7-2xxxK, i7-2xxx*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *8 MB* | [*LGA 1155*](http://en.wikipedia.org/wiki/LGA_1155) | *95 W* | [*Direct Media Interface*](http://en.wikipedia.org/wiki/Direct_Media_Interface)*, Integrated*[*GPU*](http://en.wikipedia.org/wiki/Graphics_processing_unit) | *January 2011* |
| [*Core i7-2xxxS*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29) | *65 W* |
| [***Ivy Bridge (Mobile)***](http://en.wikipedia.org/wiki/Ivy_Bridge_(microarchitecture)) | [*Core i7-3xx0QM, i7-3xx0QE*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Ivy_Bridge.22_.2822_nm.29_2) | *rPGA-988B BGA-1023* | *45 W* | [*22 nm*](http://en.wikipedia.org/wiki/22_nanometer) | *April 2012* |
| [*Core i7-3xx2QM, i7-3xx2QE*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Ivy_Bridge.22_.2822_nm.29_2) | *35 W* |
| [*Core i7-3xxxXM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Ivy_Bridge.22_.2822_nm.29_2) | *55 W* |
| [***Sandy Bridge (Mobile)***](http://en.wikipedia.org/wiki/Sandy_Bridge) | [*Core i7-2xxxXM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_2) | [*32 nm*](http://en.wikipedia.org/wiki/32_nanometer) | *January 2011* |
| [*Core i7-2xxxQM*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_2) | *6 or 8 MB* | *45 W* |
| [*Core i7-2xxxQE*](http://en.wikipedia.org/wiki/List_of_Intel_Core_i7_microprocessors#.22Sandy_Bridge.22_.2832_nm.29_2) | *6 MB* |